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MN1380 Series (CMOS LSI for Voltage Detection)

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The circuit examples given in this catalog serve merely as a guideline for product characteristics and performance.

Though this catalog has been compiled as carefully as possible, we cannot assume any responsibility whatsoever in relation to the original circuits used in the circuit examples and to third party patents. The specifications in this catalog are subject to change without prior notice due to product improvement, etc. Accordingly, please refer to the up-to-date specifications at the time of final design review.

Highly Reliable, Easy-to-Use CMOS LSIs for Voltage Detection

II OUTLINE

The MN1380 Series is a series of devices with functions for:

- · Monitoring the power supply voltage supplied to microcomputers and to LSI systems, and
- Generating the RESET signal for carrying out initialization when the power supply is turned ON, and for preventing runaway in systems when the power supply voltage fluctuates.

Recently, we have seen an increase in the number of battery-driven products such as cordless telephones, notebook-type personal computers, etc. In these products, highly accurate monitoring of the power supply voltage is an important point in terms of system operation and data backup. Moreover, with battery-driven systems such as these, the reduction of power consumed by the circuits, that monitor the power supply and detect the power supply voltage, is also an important factor in itself.

The MN1380 Series CMOS LSI is a device especially suited to this kind of application. While maintaining the voltage detection precision of similar voltage detection devices so far, the MN1380 Series of devices consumes 1/10 the current.

In addition, users can choose from one of three output formats: CMOS output, N-ch open drain and inverted CMOS output, and three types of package: the M type, TO-92 type, and surface-mounted Mini type.

With a wide range of voltage detection ranks (17 ranks from 2.0 to 4.9V), output formats, and package types, the user can choose the product most suited to his system.

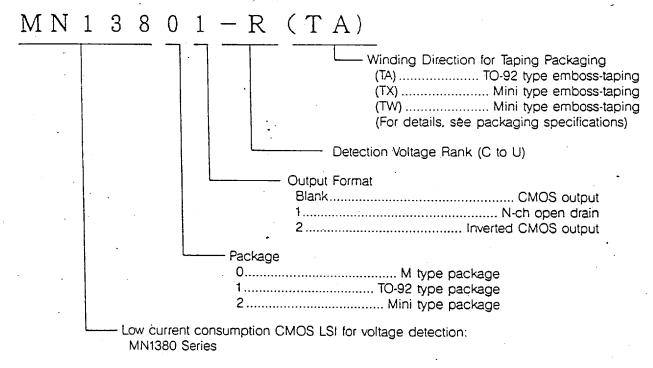
P FEATURES

- 3-pin, non-adjustment type device
- Wide selection of detection ranks (17 ranks within range 2.0 to 4.9V)
- Highly accurate detection voltage
- Detection voltage with hysteresis characteristics (ΔVD = 50mV @C to K rank, ΔVD = 100mV @L to U rank)
- Low current consumption (I DD = 1μ A type @V DD = 5V)
- Detection voltage with few changes arising from fluctuating temperature (temperature co-efficient: 1mV/°C type)
- Wide range of output formats (CMOS output, N-ch open drain, Inverted CMOS output)
- Wide selection of packages (M type, TO-92 type, surface-mounted Mini type)

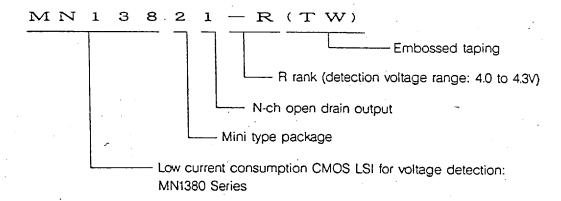
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EI NOMENCLATURE AND FUNCTIONS OF MN1380 SERIES

The MN1380 series of CMOS LSI's supports a wide range of detection ranks, output formats, packages and packaging formats. All possible combinations can be expressed in the format shown below. When ordering, please specify the desired MN1380 CMOS LSI correctly according to this format.



Example



PACKAGING QUANTITY (MINIMUM PACKAGING UNIT)

Bulk	(M type, TO-92 type, Mini type)	1000 packages
Magazine	(Mini type)	50 magazines
Taping	(Mini type, TO-92 type)	3000 tapes

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EI TYPE NUMBER LIST

Table 5.1 Type Numbers

Output	M Type	TO-92 Type	Mini Type
CMOS Output	MN1380	MN1381	MN1382
N-ch Open Drain Output	MN 1 3 8 0 1	M N 1 3 8 1 1	MN13821
Inverted CMOS Output	MN13802	MN13812	MN13822

ID DETECTION VOLTAGE RANK TABLE

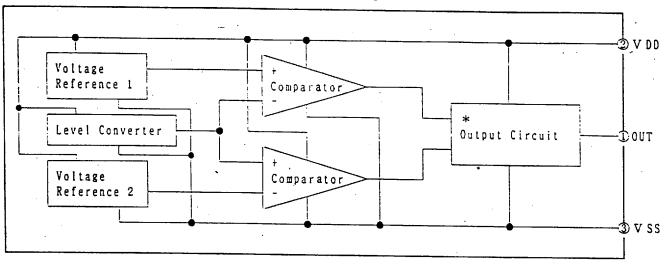
Table 6.1 Detection Voltage Rank

Rank	Detection Voltage at Drain	Supply Voltag Drop (VDL)	Unit	Detection Voltage	Hysteresis (ΔVD)	
Капк	Min.	Max.	Onic	Min.	Max.	Unit
С	2.0	2. 2	·			
D	2. 1	2.3				
E	2. 2	2.4	v	5 0	0.00	,,
F	2. 3	2.5	V	5 U ;	3 0 0	m V
G	2.4	_ 2 . 6				_
Н	2.5	2. 7				
J	2. 6	2.9	V	5 0	3 0 0	17
K	2.8	3. 1	V	5 0	3 0 0	m V
L	3. 0	3. 3				
М	3. 2	3. 5			٠.	
N	3.4.	3. 7				
Р	3.6	3. 9				
Q	3.8	4. 1	v	100	300	m V
R	4.0	4.3]			
S	4 . 2	4.5				
Т	4.4	4. 7				
U	4.6	4. 9				

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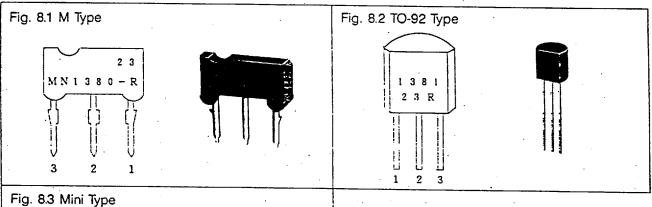
BLOCK DIAGRAM

Table 7.1 Block Diagram



* : The above circuit may vary according to the output format (CMOS, N-ch open drain, inverted CMOS drop).

II PIN CONNECTION DIAGRAM



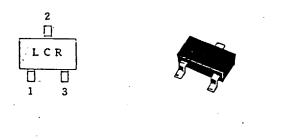


Table 8.1 Pin Descriptions

Pin	Symbol	Description
1	OUT	RESET signal output pin
2	V_{DD}	Power voltage pin
-3	Vss	Ground pin

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ABSOLUTE MAXIMUM RATINGS

Table 9.1	Absolute	Maximum	Ratings
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VSS	=	0	V	Ta	_	25°C
4 O O	-	U	٧,	ıa	=	20.0

	Item	Symbol	Rating	Unit
Αl	Drain Supply Voltage	V DD	7.0	v
A 2	Output Voltage	V o	- 0.3 ~ VDD + 0.3	v
A 3	Operating Ambient Temperature	T a	- 20 ~ ÷ 70	°C
A 4	Storage Temperature	Tstg	- 55 ~ + 125	°C

MRECOMMENDED OPERATING CONDITIONS

Table 10.1 Recommended Operating Conditions

$$VSS = 0 V$$
, $Ta = 25$ °C

Item	Symbol	Conditions	Т	olerable Lim	it	
	Cy	·	Min.	Typ.	Max.	Unit
B I Drain Supply Voltage	VDD	See Figs. 13 and 15.	1.5		6.0	. V

III DC CHARACTERISTICS

Table 11.1 DC Characteristics

$$VSS = 0 V$$
, $Ta = -20 \sim +70^{\circ}C$

, ,	Item	Symbol	Conditions		Т	olerable Lim	it	,,
	7000	Symbol		aditions	Min.	Typ.	Max.	Unit
C 1 *	Drain Supply Current	IDD	V _{DD} = 5\ Load re	r* sistance 10KΩ	·	1	5	μA
C 2	Detection Voltage at Drain Supply Voltage Drop	VDL	T Ta	= 25°C °C		_		V
C 3	Detection Voltage Hysteresis Width	△ VD	See Fig	gs. 13 and 15.		*		m V
C 4	Output Voltage, High Level	VOH	CMOS Output	I OH=-40 μ A	0.8VDD		VDD	.,,
	•		Inverted CMOS Output	V DD = 1.8V I OH = -0.5mA	0.8		VDD	V
C 5	Output Voltage, Low Level	VOL	CMOS Output N-OD Output	V DD = 1.8V $I OL = 0.7mA$	VSS		0.4	V
			Inverted CMOS Output	VDD = 6.0V $IOL = 0.3mA$	VSS		0.6	

^{*} C1: This includes output pin leak voltage

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^{*} C2 and 3: Listed by rank on page 3.

E AC CHARACTERISTICS

Table 12.1 AC Characteristics

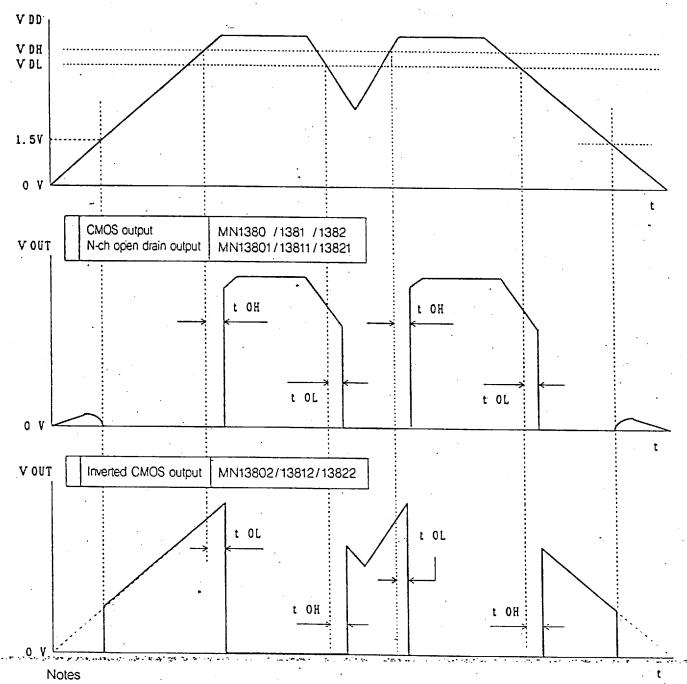
Ta = 25° C VSS = 0 V

		-			Toler	able Limit (T	Typ.)	
	Item	Symbol	Condi	tions	MN1380 MN1381	MN13801 MN13811	MN13802 MN13812	Unit
			.*	Rank	MN1382	MN13821	MN13822	
				C D E F	3. 0	•2.5	230.0	
C 6	Reset Time	t OH	See Fig.14	G H J K	3.0	3. 0	100.0	μз
				L M N P Q R S T	2.0	4.0	30.0	
				C D E F	250.0	160.0	3.0	
C 7	Reset Time	t OL	See Fig.14	G H J K	115.0	100.0	3.0	μs
				L M N P Q R S	15.0	35.0	3.0	

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E OPERATION EXPLANATORY DRAWING

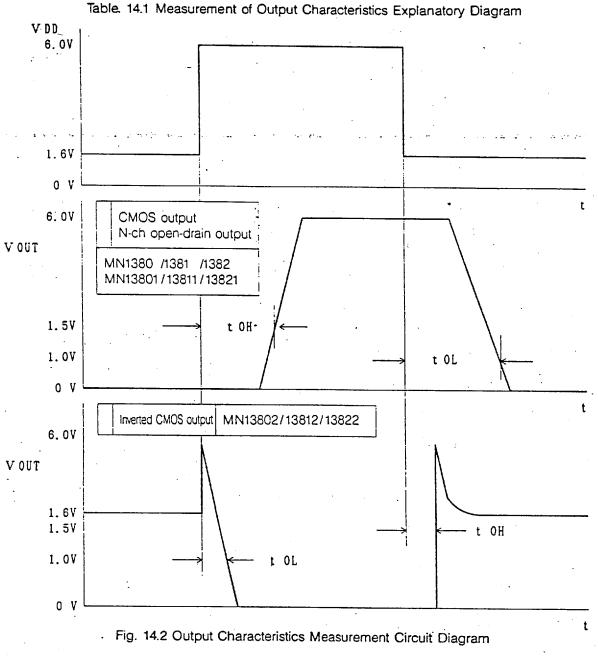
Fig. 13.1 Operation Explanatory Drawing

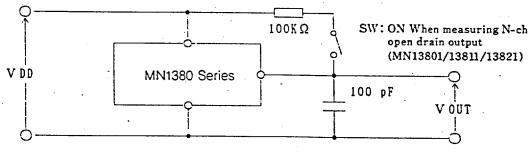


- 1. Output cannot be stipulated as operation is not guaranteed when the drain supply voltage is less then 1.5V.
- 2. VDL: Detection voltage at drop in power supply
 - V_{DH}: Detection voltage at rise in power supply
 - toL : Time from when drain supply voltage reaches detection voltage (V_{DL} or V_{DH}) up to when output (OUT) becomes Low.
 - toн: Time from when drain supply voltage reaches detection voltage (V_{DL} or V_{DH}) up to when output (OUT) becomes High
- 3. The characteristics of N-ch open drain output are the characteristics when no-load resistance is connected across the OUT and V_{DD} terminals.

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MEASUREMENT OF OUTPUT CHARACTERISTICS EXPLANATORY DRAWING





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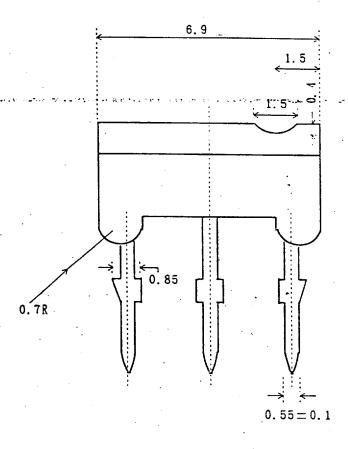
III I/O CHARACTERISTICS EXPLANATORY DRAWING Fig. 15.1 I/O Characteristics Explanatory Diagram V OUT CMOS output N-ch open drain-output MN1380 /1381 /1382 MN13801 / 13811 / 13821 \triangle V D Operation unstable/ 1.5% V DD VDL VDH V OUT Inverted CMOS output MN13802/13812/13822 Operation 1.5V V DD

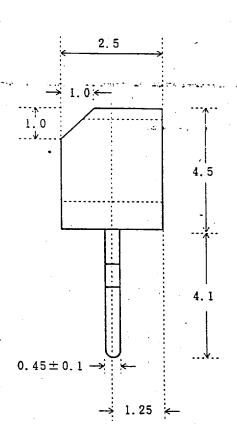
- Notes: VDL VDH

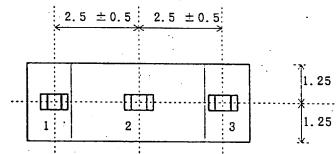
 1. Output cannot be stipulated as operation is not guaranteed when the drain supply voltage is less then 1.5V.
- VDL: Detection voltage at drop in power supply VDH: Detection voltage at rise in power supply
- The characteristics of N-ch open drain output are the characteristics when load resistance is connected across the OUT and VDD pins.
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III PACKAGE DIMENSIONS

Fig. 16.1 M Type Package Dimensions





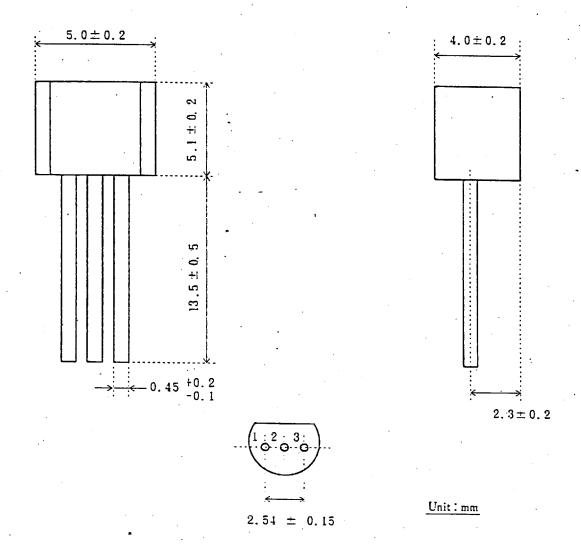


Unit: mm

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THE PACKAGE DIMENSIONS (Cont.)

Fig. 16.2 TO-92 Type Package Dimensions

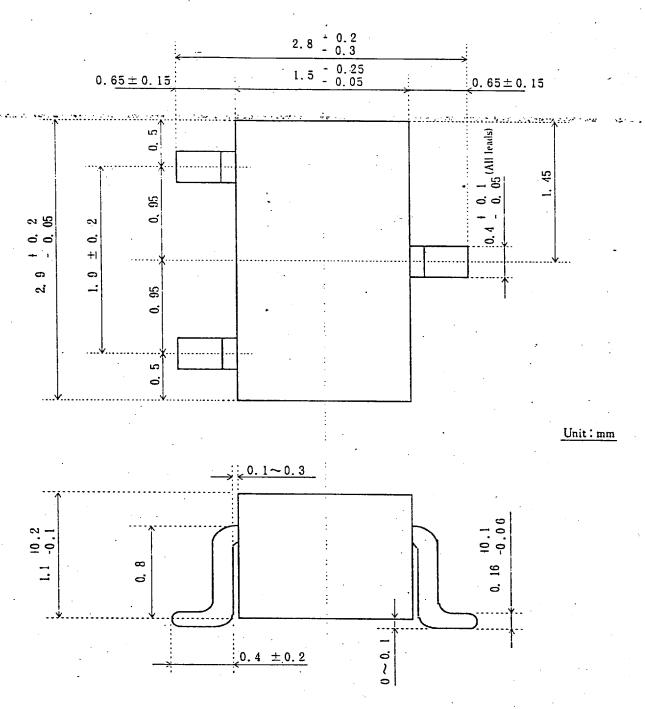


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III PACKAGE DIMENSIONS (Cont.)

Fig. 16.3 Mini Type Package Dimensions



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TREFERENCE CHARACTERISTICS DRAWINGS (Cont.)

Fig. 17.3A V_{DL}N_{DH} – Temperature Characteristics (at Q rank)

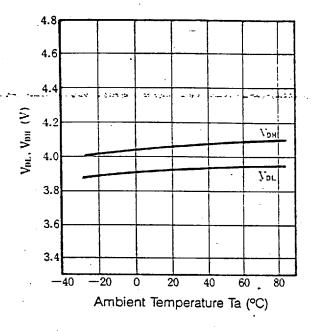


Fig. 17.38 Measurement Circuit Diagram

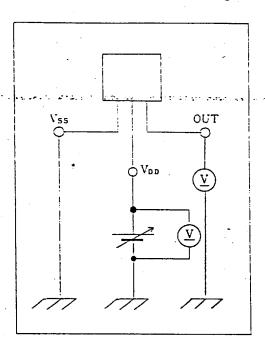


Fig. 17.4A ΔV_D - Temperature Characteristics (at Q rank)

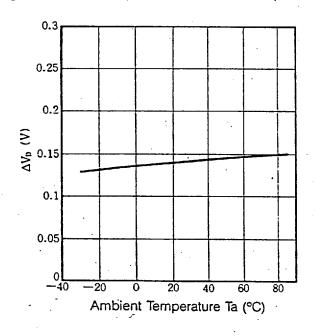
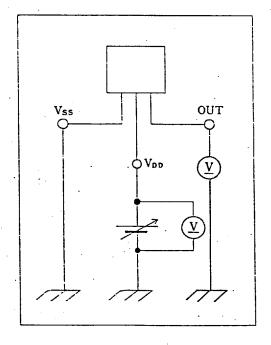


Fig. 17.4B Measurement Circuit Diagram



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TI REFERENCE CHARACTERISTICS DRAWINGS (Cont.)

Fig. 17.5A lot - Vol Characteristics

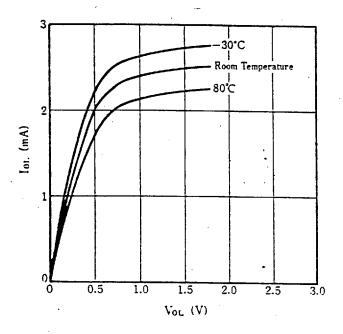


Fig: 17.58 Measurement Circuit Diagram

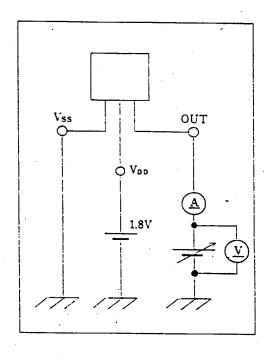


Fig. 17.6A IOH - VOH Characteristics

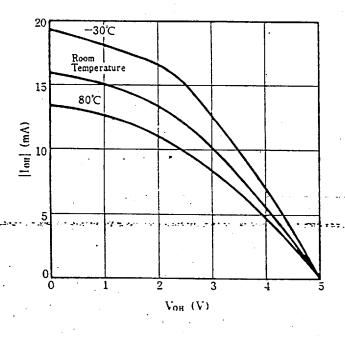
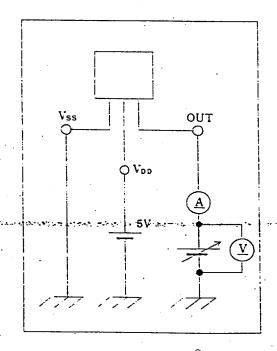


Fig. 17.6B Measurement Circuit Diagram



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TREFERENCE CHARACTERISTICS DRAWINGS (Cont.)

Fig. 17.7A lou-Temperature Characteristics

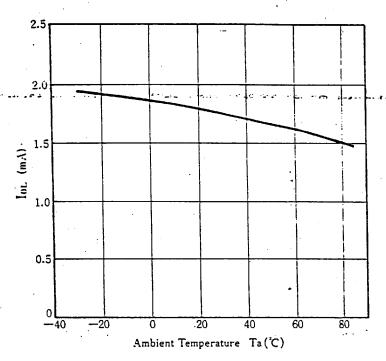


Fig. 17.7A Measurement Circuit Diagram

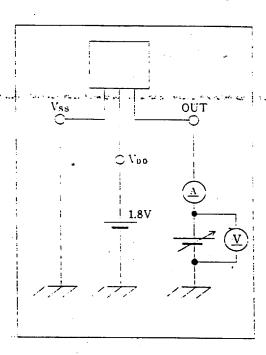


Fig. 17.8A IOH - Temperature Characteristics

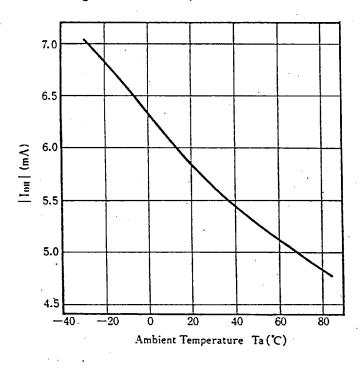
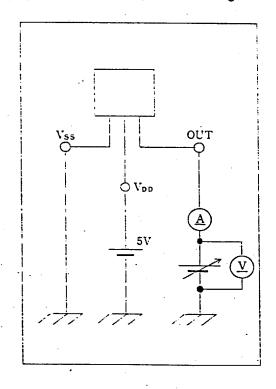


Fig. 17.88 Measurement Circuit Diagram



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MEXAMPLE OF MN1380 SERIES CIRCUIT

O Applications

- · Battery checkers
- Interrupted power detectors
- · Level discriminators
- Memory backup
- Microcomputer resetting circuits
- Resetting circuits for other electronic circuits

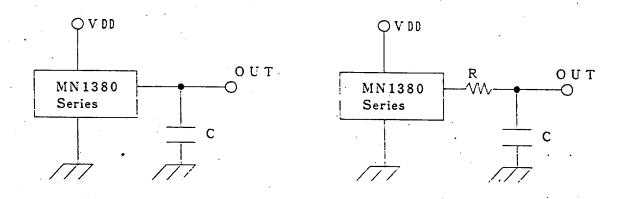
O Example of Circuit

In principle, use output pins when connecting resistors and capacitors.

Note that V_{DH} , V_{DL} and ΔV_{D} will fluctuate if a resistor is connected to the power supply pin.

Fig. 18.1 Circuit Example 1

Fig. 18.2 Circuit Example 2



Select values C and R according to the purpose for which the MN1380 Series CMOS LSI is used.

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TO-92 TYPE TAPING PACKAGING SPECIFICATIONS (MN1381/13811/13812)

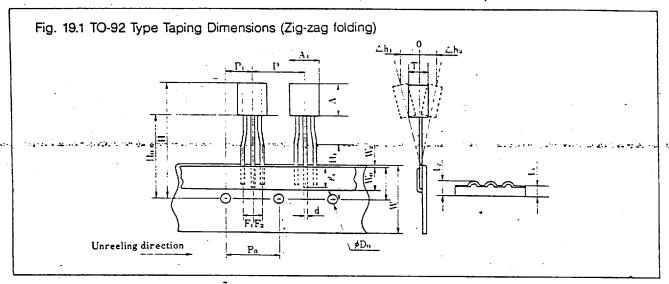


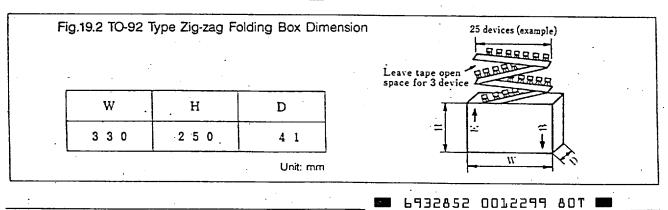
Table 19.1 TO-92 Type Taping Dimensions (Zig-zag folding)

Name	Symbol	Dimensions (mm)
Product Height*	A	5.3 шах
Product Width*	A 1	5.2 max
Product Thickness*	Т	4.2 max
Lead Width*	d	$0.45 \pm 0.15 \ -0.1$
Affixed Lead Length	<i>L</i> 1	2.0 шах
Pitch between Products	P	12.7 ± 1.0
Feed Hole Pitch	P0	12.7 ± 0.3
Feed Hole Positions	P 1	6.35±0.5
Lead Interval	F1/F2	2.5 +0.5 -0.2
Product Angling	Δ h 1 Δ h 2	2.0 max
Tape Width	. W	18.0 +1.0

Name	Symbol	Dimensions (mm)
Affixed Tape Width	W0	6.0 ± 0.5
Feed Hole Position	W 1	9.0 ± 0.5
Affixed Tape Position	W 2	0.5 max
Product Upper Surface	Н	25.0 max
Product Lower Surface	H 0	19.0 ± 0.5
Lead Clinch Height	H 1	16.0 ± 0.5
Feed Hole Diameter	D0	4.0 ± 0.2
Tape Thickness	t 1	0.7 ± 0.2
Tape Thickness (overall)	t 2	1.5 max

Note

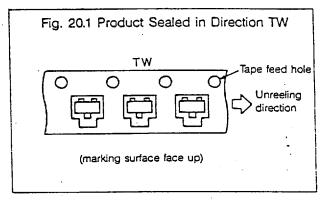
* Details are based on separate specifications.

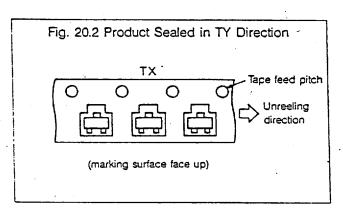


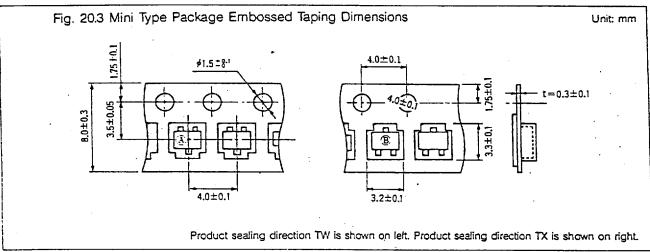
Panasonic

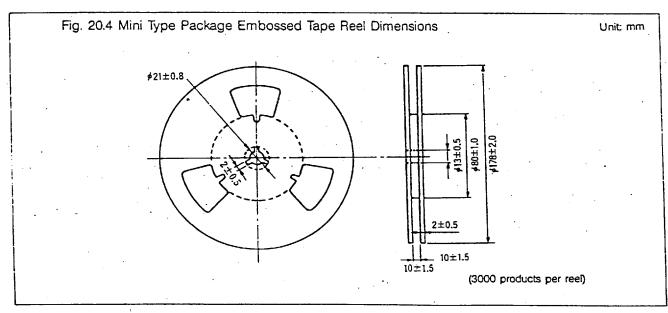
MINI TYPE EMBOSSED TAPING PACKAGING SPECIFICATIONS (MN1382/13821/13822)

O There are two taping packaging methods, TW and TX, according to the direction in which the product is inserted into the tape.









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MN1380 SERIES RELIABILITY TEST RESULTS

Table 21.1 M Type Packages (MN1380/MN13801/MN13802) TO-92 Type Packages (MN1381/MN13811/MN13812)

Test Item	Test Conditions	Results
Operating Life Test	VDD = 5.5V, Ta = 125 °C, t = 1000hrs	0 / 1 5
High-temperature Storage Test	Ta = 150 °C, t = 1000hrs	0/1,5
Low-temperature Storage Test	Ta = -65 ℃, t = 1000hrs	0 / 1 5
High-temperature, High-humidity Storage Test	Ta = 85°C、RH = 85 %、 t = 1000hrs	0 / 1 5
High-temperature, High-humidity Bias Test	VDD = 5.5∀, Ta = 85°C, RH = 85 %, t = 1000hrs	0 / 1 5
Thermal Shock Test	Ta = 150 °C ~ -65°C, 5 min each, 10 cycles	0 / 1 5
Temperature Cycle Test	T a = 150 °C ~ -65°C, 30 min each, 10 cycles	0 / 1 5
Steam Pressurization Test	2 atmospheres. 50 hrs. Ta=121°C	0 / 1 5
Solderability Test	Ta = 230 ℃, 5 sec	0 / 1 5
Solder Heat Resistance Test	Ta = 270 °C , 10 sec	0/15

Table 21.2 Mini Type Package (MN1382/MN13821/MN13822)

Test Item	Test Conditions	Results
Operating Life Test	VDD = 5.5V, Ta = 125 °C, t = 1000hrs	0 / 1 5
High-temperature Storage Test	Ta = 150 °C, τ = 1000hrs	0 / 1 5
Low-temperature Storage Test	Ta = -65 °C 、 t = 1000hrs	0 / 1 5
High-temperature, High-humidity Storage Test	Ta = 85°C、RH = 85 %、 t = 1000hrs	0 / 1 5
High-temperature, High-humidity Bias Test	VDD = 5.5V, Ta = 85°C, RH = 85 %, t = 1000hrs	0 / 1 5
Thermal Shock Test	Ta = 150 °C ~ -65°C, 5 min each, 10 cycles	0 / 1 5
Temperature Cycle Test	Ta = 150 °C ~ -65°C, 30 min each, 10 cycles	0 / 1 5
Steam Pressurization Test	2 atmospheres, 24 hrs, Ta=121°C	0 / 1 5
Solderability Test	Ta = 230 ℃, 5 sec	0 / 1 5
Solder Heat Resistance Test	Ta = 260 ℃、5 sec	0 / 1 5

^{*} Note: Note that the test conditions of Mini type packages vary with other packages.

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